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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,087	06/25/2003	Kenneth A. Bandy	BUR920020075US1	1086
23389	7590	02/17/2005		EXAMINER
SCULLY SCOTT MURPHY & PRESSER, PC 400 GARDEN CITY PLAZA GARDEN CITY, NY 11530			VINH, LAN	
			ART UNIT	PAPER NUMBER
			1765	

DATE MAILED: 02/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/604,087	BANDY ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 25 June 2003.
- 2a) This action is **FINAL**.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | Paper No(s)/Mail Date: _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>062503</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____.                                   |

**DETAILED ACTION**

***Claim Objections***

1. Claims 4, 5 objected to because of the following informalities: In lines 3 and 9 of claim 4, the word "aid" appears to be a typographical error, the examiner suggests replacing "aid" with --said--. In line 3 of claim 5, the word "aisd" appears to be a typographical error, the examiner suggests replacing "aisd" with --said--. Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 4-8, 11-12, 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al (US 6,846,618)

Hsu discloses a process for improving CD uniformity. The process comprises the steps of:

etching a first region aa' of a wafer using first etching parameters/etch variables, where a remaining portion bb' of wafer is masked/prevented from being etched (col 3, lines 18-20; fig. 4E)

etching the remaining portion bb' of a wafer using second etching parameters/etch variables, where the previously etched region aa' of wafer is masked/prevented from being etched (col 3, lines 40-43; fig. 4I)

Regarding claim 2, Hsu discloses etching the remaining portion bb' of a wafer using second etching parameters/etch variables at least one time (col 3, lines 40-43)

Regarding claim 4, Hsu discloses the steps of depositing a first layer of photoresist 44 atop the wafer, patterning the first photoresist to expose a region of the wafer where the remaining portion of the wafer is masked by the first patterned photoresist, etching the wafer while the first patterned photoresist masks the remaining portion of the wafer from etch, stripping the first patterned photoresist (fig. 3; fig. 4D-4E)

Regarding claims 5, 6, Hsu discloses the steps of depositing a second layer of photoresist 48 atop the wafer, patterning the second photoresist to expose a region of the wafer where the remaining portion of the wafer is masked by the second patterned photoresist, etching the wafer while the second patterned photoresist masks the remaining portion of the wafer from etch, stripping the second patterned photoresist (fig. 3; fig. 4H-4I)

Regarding claims 7-8, Hsu discloses etching the first area and second area with first and second etching parameters according to the properties of the first and second areas and its desired critical dimension goals (col 3, lines 19-44), which reads on

Art Unit: 1765

measuring one or more etched regions and comparing the etched regions to a predetermined specification

Regarding claim 11, Hsu discloses forming separated patterned on a wafer for improving critical dimension suitable for integrated circuits (col 2, lines 13-20), which reads on using the regions of the wafer for different chip design

Regarding claim 12, fig. 2A and fig. 2B of Hsu shows the photoresist pattern forms an etch matrix

Regarding claim 17, Hsu discloses forming a coating layer 42 atop the substrate (col 3, lines 3-4)

4. Claims 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Gardner et al (US 5,994,175)

Gardner discloses a method for manufacturing transistor comprises the steps of: implanting/doping one first region of a wafer with a first set of doping variables, where a remaining portion of the wafer is masked from being doped by a mask 130 (col 6, lines 35-50; fig. 3)

implanting/doping other region of the remaining portion of the wafer with a second set of doping variables, where the previously doped region of the wafer is masked from being doped by a mask 144 (col 7, lines 15-36; fig. 4)

Regarding claim 20, Gardner discloses the doping variables comprises: dopant species, dopant concentration and implant energy (col 6, lines 35-47)

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al (US 6,846,618) in view of Powell et al (US 6,090,717)

Hsu's method has been described above. Unlike the instant claimed invention as per claim 3, Hsu does not specifically disclose that the etch variables include etch time, tool chuck temperature and tool wall temperature although Hsu discloses that etch parameters includes temperature, bias power must be tuned (col 1, lines 24-26)

Powell, in a method for plasma etching, discloses that the etch variables include etch time, tool chuck temperature (col 10, lines 5-15)

Thus, one skilled in the art at the time the invention was made would have found it obvious to modify Hsu by includes etch variables such as etch time, tool chuck temperature and tool wall temperature as per Powell because according to Powell the

Art Unit: 1765

etching step can be optimized by varying the process parameters such as etch time, tool chuck temperature, power (col 9, lines 41-65)

7. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al (US 6,846,618) in view of Li et al (US 6,716,763)

Hsu's method has been described above. Unlike the instant claimed inventions as per claims 9-10, Hsu does not specifically disclose patterning includes transferring an image to the photoresist utilizing recticles having an opaque region

Li, in a method for controlling CD loss, discloses that patterning includes transferring an image to the photoresist utilizing recticles having opaque region (col 1, lines 40-45; fig. 5)

Thus one skilled in the art at the time the invention was made would have found it obvious to modify Hsu patterning step by including transferring an image to the photoresist utilizing recticles having opaque region as per Li because Li discloses that the formation of semiconductor structure typically requires of such structure in a layer of photoresist by exposing the photoresist with light passing through a reticle containing the desired pattern (col 1, lines 35-44)

8. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al (US 6,846,618) in view of Gale et al (US 4,155,627)

Hsu's method has been described above. Unlike the instant claimed inventions as per claims 13-16, Hsu does not specifically disclose that the first and second photoresist

Art Unit: 1765

pattern are line stripe of photoresist having a stripe width and etching the stripe of photoresist to decrease the line stripe width

Gale discloses a method for forming multi-level pattern comprises the step of forming line stripe of photoresist having a stripe width and etching the stripe of photoresist to decrease the line stripe width (col 8, lines 40-51; fig. 4)

One skilled in the art at the time the invention was made would have found it obvious to modify Hsu method by forming line stripe of photoresist having a stripe width and etching the stripe of photoresist to decrease the line stripe width to provide a desired two-level relief pattern of specified depth in the substrate as taught by Gale (col 9, lines 1-4)

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al (US 6,846,618) in view of Singh et al (US 6,191,046)

Hsu's method has been described above. Unlike the instant claimed invention as per claim 18, Hsu does not specifically disclose the step of reworking the first layer of photoresist prior to depositing the secondary photoresist

Singh discloses a method for reworking a photoresist comprises the step of reworking the first layer of photoresist prior to depositing the secondary photoresist (col 6, lines 10-15; 64-67)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Hsu's method by adding the step of reworking the first layer of photoresist prior to depositing the secondary photoresist as per Singh because Singh

discloses that reworking or re-patterning a photoresist is economically desirable, as compared to scrapping the wafer, when there is one correctly formed lower layer already formed beneath a photoresist layer (col 1, lines 40-43)

### ***Conclusion***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471.

The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



LV  
February 15, 2005